AUTOMATIC OPERABILITY RESTORATION OF SEMICONDUCTOR MEMORY'S MODULES DURING MULTIPLE FAULTS

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ABSTRACT

A structure of the memory modules with built-in self-test and recovery means, which will perform the replacement of data bits of the main memory cell array in which faults were accrued at the output data from the spare memory cell array, is proposed. The automatic reconfiguration of the memory structure, while faults detection, provided by the suggested hardware and software means. Implementation of self-testing semiconductor memory modules with recovery efficiency at multiple faults can substantially reduce the cost and increase the rate of fault coverage, as the self-test takes place on the operating frequencies and thus does not require external test bench equipment. Semiconductor memory modules with automatic recovery functionality at multiple faults can be used in systems of critical applications protection and management where the use of fault-tolerant digital devices is a necessity due to the inability of traditional methods of repair by replacing the failed elements. For critical application systems, which control nuclear power plants and other energy facilities, air, sea and ground vehicles, the needs to ensure their operability are increased. To fulfill this requirement, it is necessary to increase the technical readiness coefficient, the value of which increases with decreasing recovery time control system in case of fault of its constituent units. The main control system components critical applications are memory devices, which store programs and used for performing algorithms control. RAM is one of the most reliable components of the computer, because manufacturers of memory modules carefully tested its products before they hit the market as finished products. However, in memory circuits due to static electricity, the migration of electrons because of the high conductivity oxide, the tunnel effect, etc. over the time, there may be faults due to the instability of the charges.

Keywords: Storage devices, built-in, self-test, operability restoration.

INTRODUCTION

At using the RAM for error checking, it is recommended to apply widespread utility Memtest86+. However, when testing memory modules having this utility idle cycles during which memory components recovery may occur, however such a mode divergence may give inaccurate testing results.

If testing found inefficient units, they should be replaced by serviceable. However, the time spent searching for the same memory module and to check the validity of the timing, as indicated in SPD. Significant time required to restore the system may lead to irreparable consequences for critical application systems.

Memory type ECC (Error Check & Correction/Error Correction Code), is able to automatically correct any single error and detect any dual. As long as the memory is functioning more or less normally, the opposition of entropy and a noise codes resolved in

favor of the latter. However, the full or partial output of one or more memory modules fail, corrective ability of controlling codes are not enough and memory begins to work very unstable.

LITERATURE REVIEW

The known system with replacing rows and columns analyzing of internal memory for spares, which comprises a built-in self-test means (BIST), built-in recovery analysis (BIRA) performance means, switched the address codes, and data operations, the main memory cell array, spare rows and columns of cells, decoders of rows and columns of cells [1]. The disadvantage of this system is limited functionality due to a limited number of spare memory cells, which does not allow to carry out repairs at the component faults that cause inoperable whole discharge data. Also repair and restore an operability state of memory circuits during their operation is impossible.

The general approach of BIST for memory circuits includes the introduction of chip circuitry to generate additional tests, comparison and synchronization of responses with reference data. Typical structure of the memory chip with built-in self-test is shown in Figure 1 and comprises a controller, addresses and data code generator, data comparator and switches, providing connection to the array of memory cells signals in the operation or test mode [2].
Using BIST architecture is cost-effective in the long term, by 2018, according to the SIA, 90% of silicon will be with integrated self-diagnostics, so that efforts must be focused on self-test embedded systems using programmable built-in resources.

When modifying BIST architecture is necessary to ensure rapid switching of the test process in the normal operation of the chip. Coverage of possible faults should increase with increasing period of operation chip, with hardware costs must be as low as possible, so as not to greatly increase the cost of implementing the new architecture. The memory chips with built-in self-repair (BISR) developers typically use spare rows and/or columns of cells replacement [3-5].

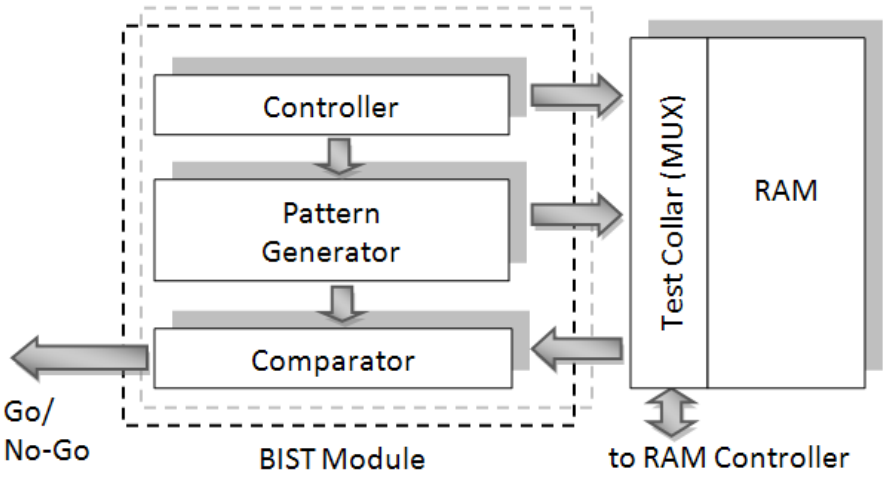

FIG.1. Typical structure of a memory chip with built-in self-test

In memory modules of modern personal computers these days the Hamming code is used (n,k), single error correction and double error detection. Use of error-correcting codes, requires the implementation of schemes operating in real time.

Suppose in k information bits $m_1, m_2, \ldots, m_k$ added r check bits to form a code word length $n = k + r$. Each check bits generated independently of other verifying bits and is generated by a linear combination of information resources.

$$c_1 = h_{11}m_1 \oplus h_{12}m_2 \oplus \ldots \oplus h_{1k}m_k,$$
$$c_2 = h_{21}m_1 \oplus h_{22}m_2 \oplus \ldots \oplus h_{2k}m_k,$$
$$\ldots$$
$$c_r = h_{r1}m_1 \oplus h_{r2}m_2 \oplus \ldots \oplus h_{rk}m_k.$$

A code word read from memory n - bit vector $V = (v_1, v_2, \ldots, v_n)$, is considered correct at the following condition:

$$\mathbf{H}V^{\mathbf{T}} = 0, \quad (1)$$

where $V^{\mathbf{T}}$ – transposed vector V, $\mathbf{H}$ – check matrix. The summation is performed in module 2. The check matrix $\mathbf{H}$ is represented as

$$\mathbf{H} = |\mathbf{P}, \mathbf{I_r}|, \quad (2)$$

where $\mathbf{P}$ – binary matrix of dimension $r \times k$, a $\mathbf{I_r}$ – the single matrix of dimension $r \times r$.

The first k bit code word are information bits, r – the last – control.

The word, read from the memory may differ from the written word. If $\mathbf{U}$ – a code word that is written in the memory, and V – the resulting vector, then $\mathbf{E} = V - \mathbf{U} = (e_1, e_2, \ldots, e_n)$ it called vector error. Checking the read word consists in calculating error syndrome:

$$\mathbf{S} = \mathbf{H}V^{\mathbf{T}} = V\mathbf{H}^{\mathbf{T}} = (\mathbf{U} + \mathbf{E}) \cdot \mathbf{H}^{\mathbf{T}}.$$

If $\mathbf{S}$ – the zero vector, it is considered that there are no errors. Otherwise syndrome defines the error vector. The syndrome is the sum of the columns h of the matrix $\mathbf{H}$, which corresponds to the error. If the column h_i zero error at that position code word will have no impact on the syndrome, and will not allow detecting an error. If two columns of $\mathbf{H}$ matrix were the same, the single error in each of these code positions, give the same syndrome. Figure 2 shows a diagram of the error detection and correction device of PC memory.

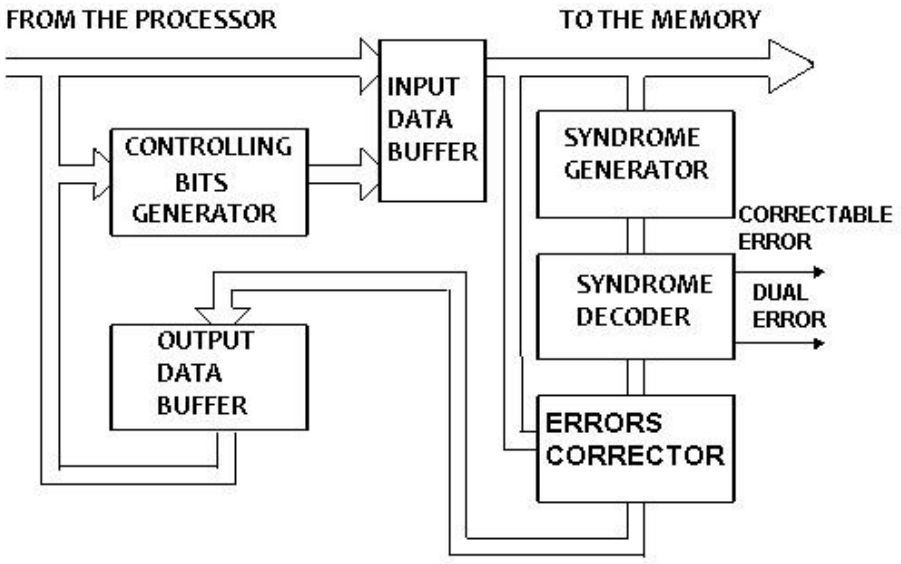

FIG.2. Diagram of the error detection and correction device of PC memory

The scheme consists of a bits control generator, data buffers, syndrome generator, a syndrome decoder and error corrector. To the data bits the data bits controllers are added, formed according to the Hamming code. The data via the first buffer move to write inputs of memory chips.

The read data is move to the control on the syndrome generator. Syndrome decoder generates a signal “Correctable error”, which is usually used to start the interrupt handler, fixing the amount and intensity of the occurrence of single errors. Signal “Fatal error” generated by syndrome decoder, used to enable the hardware interrupt “Memory error”. With the help of Hamming codes only single error can be corrected, but the functionality of the memory with a few faults cannot be recovered.

METHODOLOGY

In order to eliminate the disadvantages mentioned above, it’s proposed to include in the memory module an array of free data bits, which allows to record, store and retrieve data designed for storing in one or more data bits that are basically faulted the memory array. Upon detection of multiple faults the reconfiguration the structure of the memory module will be provided automatically instead of adding new hardware and software [6-17]. A block diagram of a memory module with efficiency automatic recovery under multiple faults is shown in Figure 3.

The memory module includes a primary and backup storage arrays, the controller self-test and efficiency recovery, address code generators and data multiplexers of operation codes, address and data comparator, input and output data reconfigurator, efficiency recovery unit.
The implementation the embedded self-test significantly reduces the cost and increases the percentage of fault coverage, as it scans the operating frequencies and doesn’t require an external test equipment, the cost of which is usually many times higher than the cost of the memory itself.

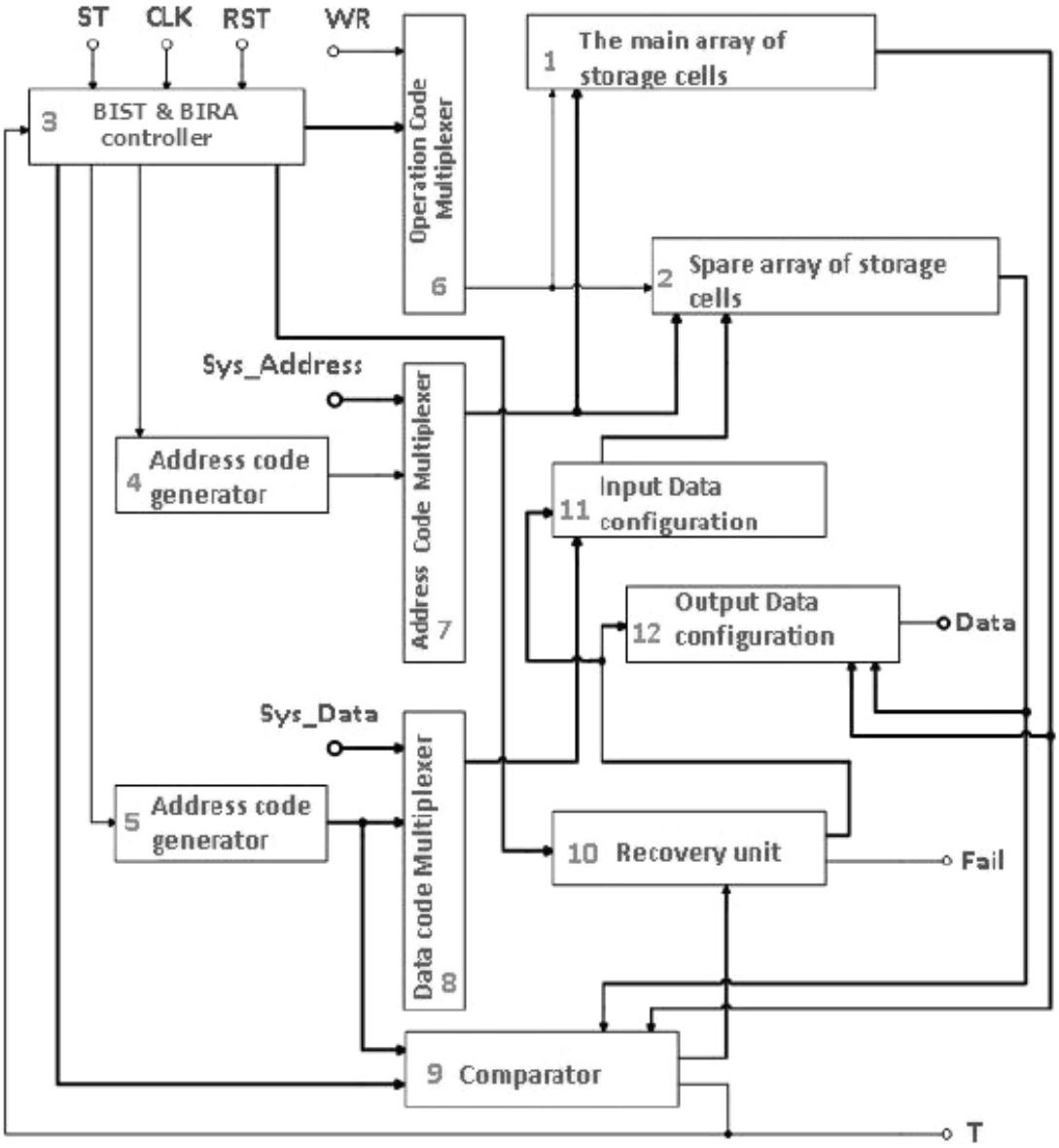

FIG.3. Block diagram of a memory module with efficiency automatic recovery under multiple faults

RESULTS

ECC memory modules can detect and restore only the data bits, controlling bits are not subject to correction. Then, for example, for 64 data bits a single fault is allowed, and not for the 8 control bits. In this case, the probability of faults of the module with ECC is equal to the sum of the probabilities of faults of dual 64 data bits and the probability of faults of a single 8 controlling bits. Graphs of the probability of faults of the memory module: q(t) – without using the proposed method; q1(t), q2(t), q3(t) и q4(t) – in carrying out 1, 2, 3 and 4 repairs are shown in Figure 4. Also in red in Figure 4 shows the probability of correct operation of the memory module without repair – p(t), in black the probability of double faults of 64 and single fault of 8 controlling bits of the memory module – q5(t).

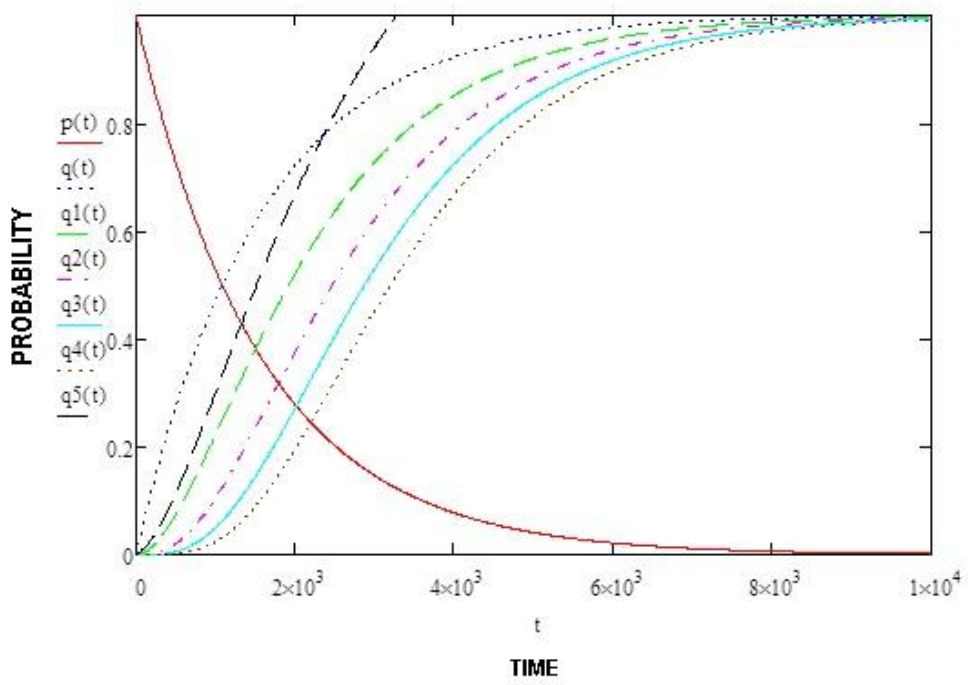

FIG.4. Graphs of faults probability of the memory module

The histogram of the probability of faults of the memory module is presented in Figure 5.

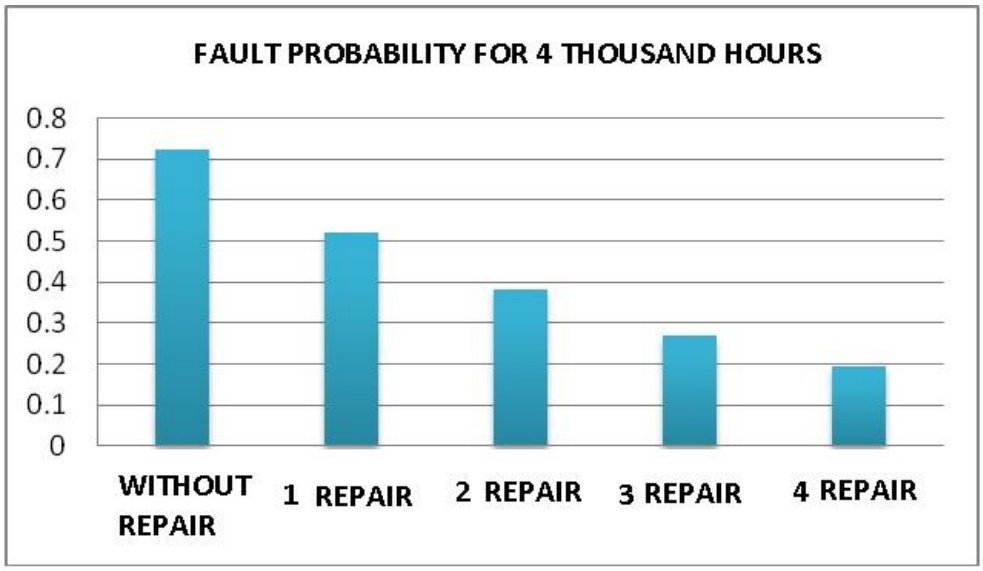

FIG.5. Histogram of the probability of faults of the memory module

From the Figure 5 we can see that in carrying out four repairs, the probability of faults is reduced by 3.7 times compared with the module, where the repair is not performed. During the product's architecture designing, it's ensured to have highly diagnostic properties of the generated tests. This reduces the capacity of the test program by utilizing hardware and firmware method of tests forming that combines high performance with low hardware costs. For example, the duration of memory chips test with a capacity of 640 Mbps and with a circulation time of 20 ns via the proposed product is 1.

In the product a multiprocessor structure of the device of diagnosing test of semiconductor memory products is used and a method of micro operations parallelization in tests algorithms. The development of tests programs is carried out in the system of specialized interpreting programming language Prover, while ensuring the mobility of tests programs at change of parameters of the diagnosed products. To reduce the cost of products are used the instrumental tools of development and debugging the programs of models verification of high-speed semiconductor memory chips, ensuring a clear and easy way of the modeling results presenting: a translator of the language Prover into VHDL language and a program of modeling results visualization.

CONCLUSIONS

Multiple increasing in the reliability of the control and information computer systems, which is especially important for critical applications systems, including the space equipment, aircraft equipment and other aerial devices. Repair of storage control systems of unmanned aircraft will be possible in automatic mode without the participation of the staff. This reduces the capacity of the programs test by utilizing hardware and firmware method of test forming that combines high performance with low hardware costs. The weight of storage devices is reduced by duplicating not the whole product, but only a part of its constituent components.

Manufacturers of storage devices are proposed to purchase a manufacture license of memory modules with built-in tools that provide automatic efficiency recovery during multiple faults. Universities and colleges can buy diagnostic software of storage devices including: interpretive language system Prover, program of micro operations parallelization in programs test Transfor.exe, test program generator for a given capacity of memory chips Testgen.exe, language translators from Prover into VHDL and Active-VHDL, modeling results visualization program, program of interpreting, visualization and analysis (IVA) of the results of modeling, software of optimized test sequence selection Optim.exe.

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